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Implementation of Coordinate Rotation algorithm for Hardware Multipliers

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Abstract*— Most of the hardware algorithms exist to handle the hardware intensive signal processing problems. Among these algorithms is a set of shift-add algorithms collectively known as CORDIC for computing a wide range of functions including certain trigonometric, hyperbolic and logarithmic functions. Apart from this it can handle linear functions. Even though numerous articles covering various aspects of CORDIC algorithms, very few surveys concentrate on implementation in FPGAs. CORDIC (Coordinate Rotation Digital Computer) is an algorithm for computing transcendental functions like sine, cosine and arctangent. The method can also be easily extended to compute square roots as well as hyperbolic functions. The algorithm works by reducing the calculation into a number of micro-rotations for which the arctangent value is precomputed and loaded in a table. This method reduces the computation to addition, subtraction, compares, and shifts.Various digital architectures were proposed and compared, including low-cost sequential and high performance pipelined solutions. Fixed point and floating point arithmetic was considered. The concepts were implemented in VHDL, verified and synthesized with Xilinx tools. Selected approach was physically implemented and tested.

Index Terms*— CORDIC, sine, cosine, FPGA, synthesis. SVD, digital, hardware, VHDL, FPGA

I. INTRODUCTION

In 1959 Jack E. Volder described the Coordinate Rotation Digital Computer or CORDIC for the calculation of trigonometric functions, multiplication, division and conversion between binary and mixed radix number systems. The CORDIC- algorithm provides an iterative method of performing vector rotations arbitrary angles using only shift and add. Processing of matrices, especially inversion remains a key challenge for contemporary computing machines. Very smart algorithms were proposed many years ago, by the scientists who expected rapid development of digital hardware in the future. Many of those solutions were presumed to work on futuristic parallel devices. CORDIC are good examples here [1-3]. Eventually recent years have brought the long expected rapid development of digital hardware and growth of programmable logic devices complexity. This paper describes a study of hardware implementation and theory on CORDIC modules. The authors focus on comparison of architecture variants in the context of resource allocation, speed and accuracy. Similar works may be found in contemporary literature [8] showing growing interest in practical use of achievements of great mid 20-th century mathematicians.

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II. CORDIC THEORY

To rotate the coordinate (X i ,Y i) to the point (Xj,Yj) We use the following matrix calculation.

$$\begin{bmatrix} X_j \\ Y_j \end{bmatrix} = \begin{bmatrix} \cos\Theta & -\sin\Theta \\ \sin\Theta & \cos\Theta \end{bmatrix} * \begin{bmatrix} X_i \\ Y_i \end{bmatrix} \quad (1)$$

Equation 1 can be modified by factoring a cos□ leading to the following:

$$\begin{bmatrix} X_j \\ Y_j \end{bmatrix} = \cos\Theta * \begin{bmatrix} 1 & -\tan\Theta \\ \tan\Theta & 1 \end{bmatrix} * \begin{bmatrix} X_i \\ Y_i \end{bmatrix} \quad (2)$$

Any angle Θ in the first quadrant can be represented by the following equation.

$$\Theta_n = \sum_{n=0}^{\infty} S_i * \arctan\left(1/2^n\right) \quad (3)$$

where Si = 0 or 1

For example, the angle 0 is computed by letting S_i in equation (3) be simply Si =0,0,0,0... . The angle Θ =π/2 is computed by letting S i =1,1,1,1... . π /4 would be 1,0,0,0... , and so on. In practice, due to the accuracy limits of the digital representation, the summation can be limited to the number of bits representing the value, or fewer. The arctan(1/2)^n quickly approaches 0.

Note that equation 3 can also be constructed such that S_i = -1 or 1. For example, the angle π /4 would be computed with the sequence 1,1,−1,−1,−1,... . The advantage of this method will become apparent. This results in the following equation for $\tan\Theta_n$.

$$\tan\Theta_n = S_n * (1/2^n) \quad (4)$$

Turning our attention back to equation (2), and given that the angle Θ can be represented as a weighted sum (3), we can represent the rotation from (X i ,Y i) to (X j ,Y j) as a sequence of smaller rotations where the n+1 rotational coordinate is derived from the n th coordinate using the following equation

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \cos\Theta_n * \begin{bmatrix} 1 & -\tan\Theta_n \\ \tan\Theta_n & 1 \end{bmatrix} * \begin{bmatrix} X_n \\ Y_n \end{bmatrix} \quad (5)$$

By substituting equation (4) into equation (5) we replace the tangent function with a divide by 2^n , which is a simple shift operation

$$\begin{bmatrix} X_{n+1} \\ Y_{n+1} \end{bmatrix} = \cos\Theta_n * \begin{bmatrix} 1 & -S_n * (1/2^n) \\ S_n * (1/2^n) & 1 \end{bmatrix} * \begin{bmatrix} X_n \\ Y_n \end{bmatrix} \quad (6)$$

By implementing the algorithm letting S_n take on the values -1 and 1, and by noting that

$$\cos(\Theta) = \cos(-\Theta) \quad (7)$$

the $\cos(\Theta)$ term reduces to a constant K given by the equation

$$K=\prod_{n=0}^{\infty}\left(\cos\left(\arctan\left(1/2^{n}\right)\right)\right)\approx 0.607253 \qquad (8)$$

The constant K means that the CORDIC function as an overall gain by the factor 1/K which is often referred to as the CORDIC gain. Since this is a constant, it can be taken into account in other parts of the system.

The CORDIC algorithm can be implemented in hardware using three approaches: a sequential approach - the structure is unfolded in time, a parallel approach – the structure is unfolded in space or a combination of the two. In the first-sequential approach, arithmetic modules are shared by iterations. Intermediate results are fed back via the registers and the appropriate angles are delivered to arithmetic units by the muxes. Control is provided by iteration counter. Figure 1 shows the CORDIC sequential architecture.

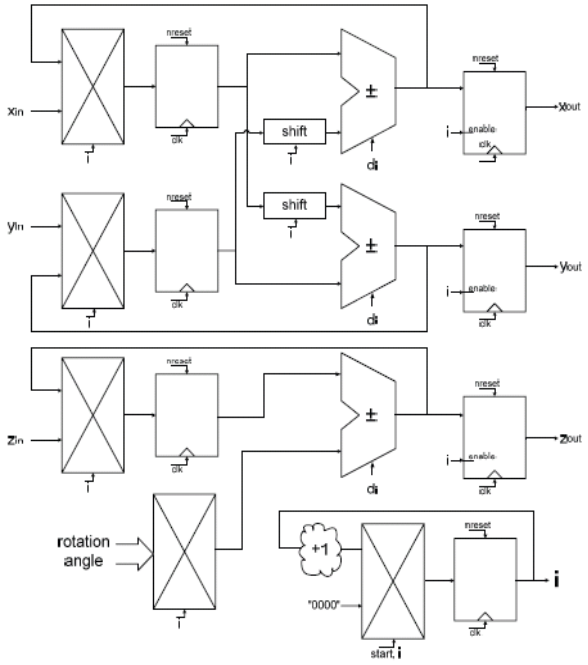


Figure 1. CORDIC - sequential architecture

Another concept is pipelined architecture presented in Fig. 2. Schematic shows a hardware providing 3 consecutive iterations. Arithmetic blocks are replicated for each iteration, thus the data flow may form a pipeline. This solution provides much faster throughput but needs more hardware resources. Arithmetic is fixed point with 8-bit numbers coded in 2'complement *Figure 3 shows the CORDIC hardware implementation*

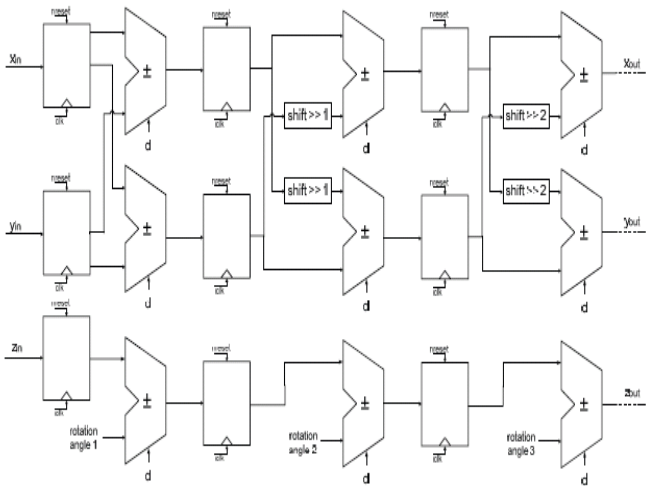


Figure 2. CORDIC – pipelined architecture

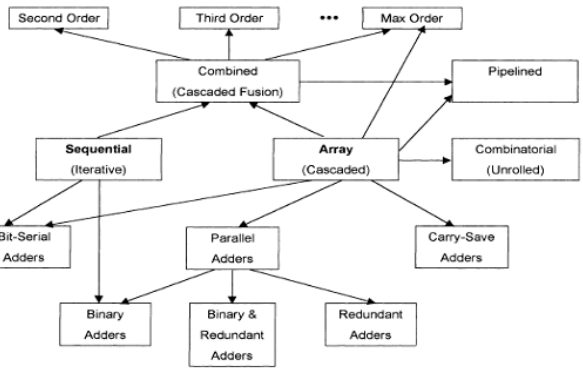


Figure 3: shows the CORDIC hardware implementation.

III. IMPLEMENTATION RESULTS

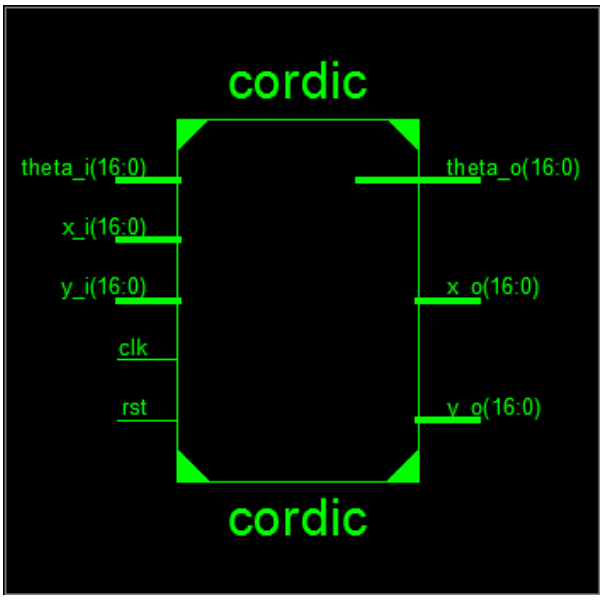


Fig. 4 shows the RTL block of the cordic algortihm

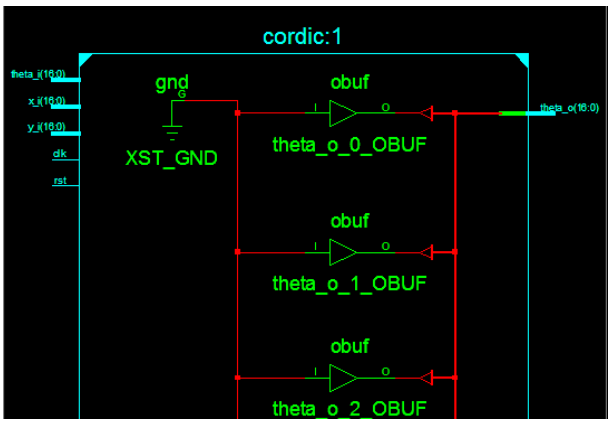


Figure 4 shows the technology schemeatic.

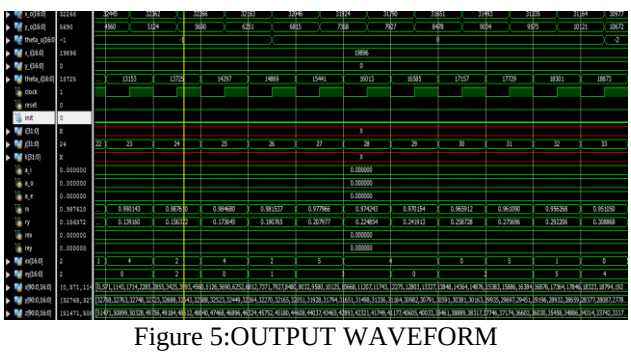


Figure 5:OUTPUT WAVEFORM

IV. CONCLUSIONS

This paper presents theoretical and practical aspects of implementing sine/cosine CORDIC-based generators in FPGAs. The main results can be summarized as follows: A trade-off speed/area will determine the right structural approach to CORDIC FPGA implementation for an application. Module count and operating speed depend significantly on the used synthesis tool. Simulation has shown that the redundant adder can improve the efficiency of CORDIC FPGA implementations for bit-lengths higher than 32-bit.

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